PROJECT WHIRLWIND

Angelo Papenhoff/aap
aap@papnet.eu

Computers in the 1940s

- human computers: lady at a desk
- punch card equipment: accounting &c.
- differential analyzers: solve differential equations mechanically
- electromechanical (relay) digital computers:
  - Zuse Z3
  - Harvard Mark I (essentially Charles Babbage's Analytical Engine)
  - IBM SSEC (IBM's successor to Mark I)
- electronic (vacuum tube) digital computers:
  - Colossus (classified until 70s, irrelevant to the field)
  - ENIAC (built to compute ballistic tables)
  - EDVAC (successor to ENIAC, *the* von Neumann computer)
  - EDSAC (inspired by EDVAC)
  - IAS Computer (roughly contemporary with Whirlwind)
  - but: not even finished when Project Whirlwind starts

Computers in the 1940s

- how to steer the calculation?
  - hardwired (analog computers, ENIAC initially)
  - coded program from cards/tape (electromechanical computers)
  - coded program in storage (electronic computers, ENIAC later)
- storage/memory technology
  - only registers
  - delay line (EDVAC, EDSAC)
  - storage tubes (Manchester Baby, 1948, IAS machine)
  - ...
- serial vs. parallel: mostly tied to storage technology
- number base
  - decimal (ENIAC, Mark I, SSEC)
  - binary (Z3, EDVAC, EDSAC, IAS machine)
- number of digits
  - Z3: 22 binary digits, floating point(!)
  - usually: ~10-12 decimal digits or binary equivalent (30-40)

Pre-history of Project Whirlwind

- 1943/4
- Problem: training flight crews on warcraft costs too much time and money
- Solution: ground-anchored flight trainers
- flight trainers went from pneumatic to electric (analog)
- But: new trainer for every aircraft
- Captain Luis de Florez (MIT):
- Airplane Stability and Control Analyzer (ACSA): universal flight trainer that can be configured to simulate various airplanes
- flight simulators had been built at Bell Labs
- ACSA goes to MIT's Servomechanisms Lab (Gordon Brown)

Aircraft analyzer

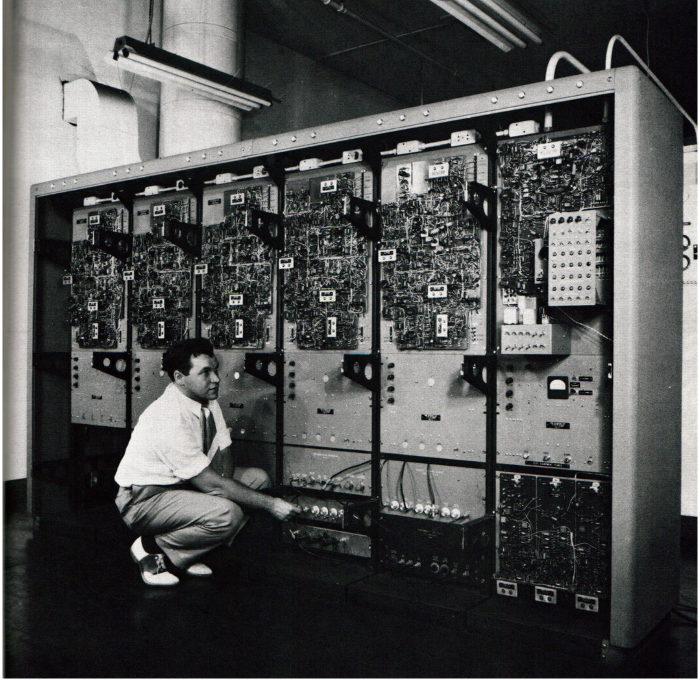
- 1944/5
- end of 1944: preliminary study of the analyzer to determine feasibility
- cockpit + analog computer (mechanical or electrical)
- Jay Forrester becomes director of the project and brings in Robert Everett
- study existing flight trainers and physics behind them
- at least 47 equations of 53 variables
- analog computer: electromechanical differential analyzer
- turns out to be more complex and difficult than anticipated
- Forrester learns about digital computers from Perry Crawford in late summer of ’45

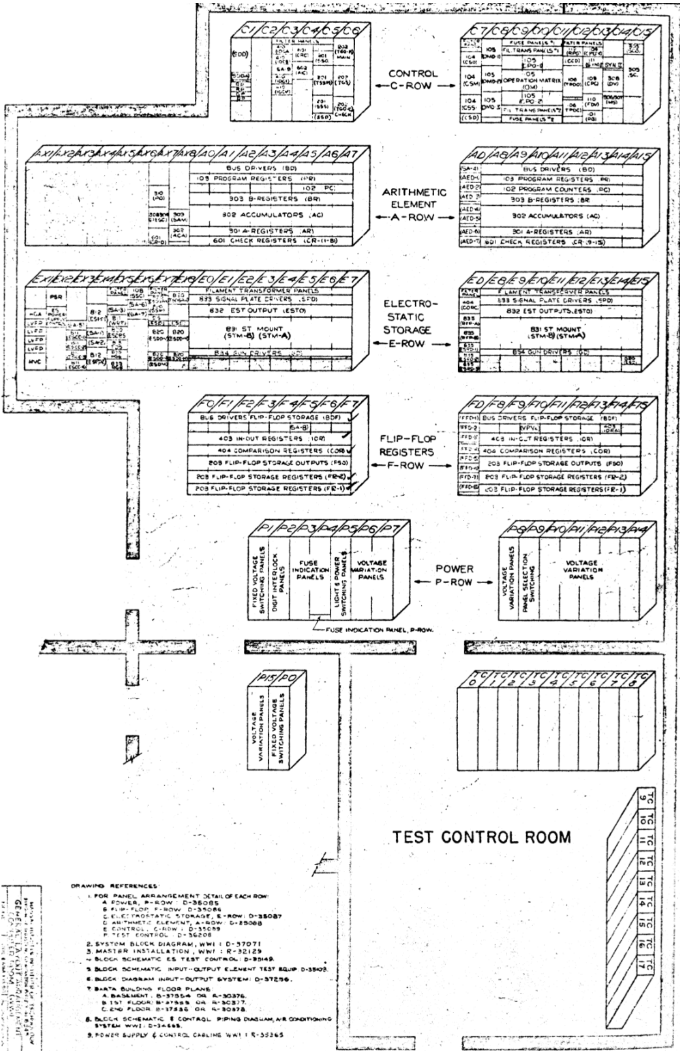
Digital computers

- End of '45: explore digital approach to aircraft analyzer's problems
- has to be electronic to be fast
- binary number system to be preferred
- rewards: more reliable, higher accuracy, lower cost, smaller size, more flexible, application to other problems than aircraft analysis
- possible military applications:
  - aircraft stability and control
  - automatic radar tracking and fire control
  - stability and trajectories of guided missiles
  - study of aerial and submarine torpedos
  - servomechanisms systems
  - stability and control characteristics of surface ships
- early '46: Project Whirlwind
- Phase I: construct small digital computer [...]
- Phase II: build aircraft analyzer based on Phase I

Digital computer

- investigate:
  - block diagrams
  - computing circuits
  - mathematics
  - mechanical questions, including cockpit
  - mercury delay lines
  - storage tube research
  - other electronic problems
- serial or parallel?
- delay line or storage tube memory?
- how many bits?
- ...
- sept. 1947: Whirlwind I Computer Block Diagrams (R-127)
- late 1948: no more Phase II, cockpit scrapped
- 5-digit multiplier built to test circuitry and reliability

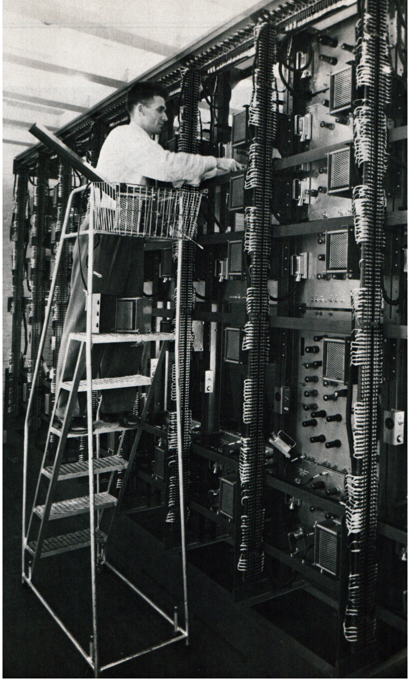




DRAWING REFERENCES:

1. FOR PANEL ARRANGEMENT DETAIL OF EACH ROW:
   - A POWER, P-ROW: D-35085
   - B FLIP-FLOP, F-ROW: D-35086
   - C ELECTROSTATIC STORAGE, E-ROW: D-35087
   - D ARITHMETIC ELEMENT, A-ROW: D-35088
   - E CONTROL, C-ROW: D-35089
   - F TEST CONTROL: D-36208
2. SYSTEM BLOCK DIAGRAM, WWI: D-37071
3. MASTER INSTALLATION, WWI: R-32129
4. BLOCK SCHEMATIC ES TEST CONTROL: D-35149.
5. BLOCK SCHEMATIC INPUT-OUTPUT ELEMENT TEST EQUIP: D-35103.
6. BLOCK DIAGRAM INPUT-OUTPUT SYSTEM: D-37256.
7. BARTA BUILDING FLOOR PLANS:
   - A. BASEMENT: B-37554 OR R-30376.
   - B. 1ST FLOOR: B-37555 OR R-30377.
   - C. 2ND FLOOR: B-37556 OR R-30378.
8. BLOCK SCHEMATIC & CONTROL PIPING DIAGRAM, AIR CONDITIONING SYSTEM WWI: D-34665.
9. POWER SUPPLY & CONTROL CABLING WWI: R-35365

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
GENERAL LAYOUT ARRANGEMENT
COMPUTER ROOM - WWI




Difficult times

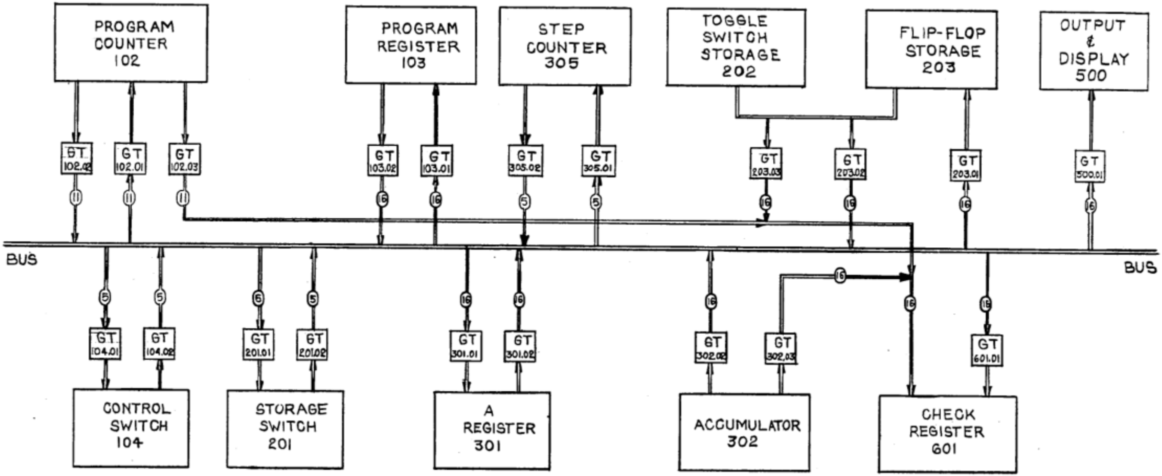
- Project is in trouble 1946-1950
- "peace broke out" $\rightarrow$ bad times for funding of military projects
- what is the purpose of Whirlwind?
- way too expensive, and for what?
- ONR complained about lack of mathematical insight
- ONR didn't understand computer engineering
- Air Force wants air defense system, saves the project

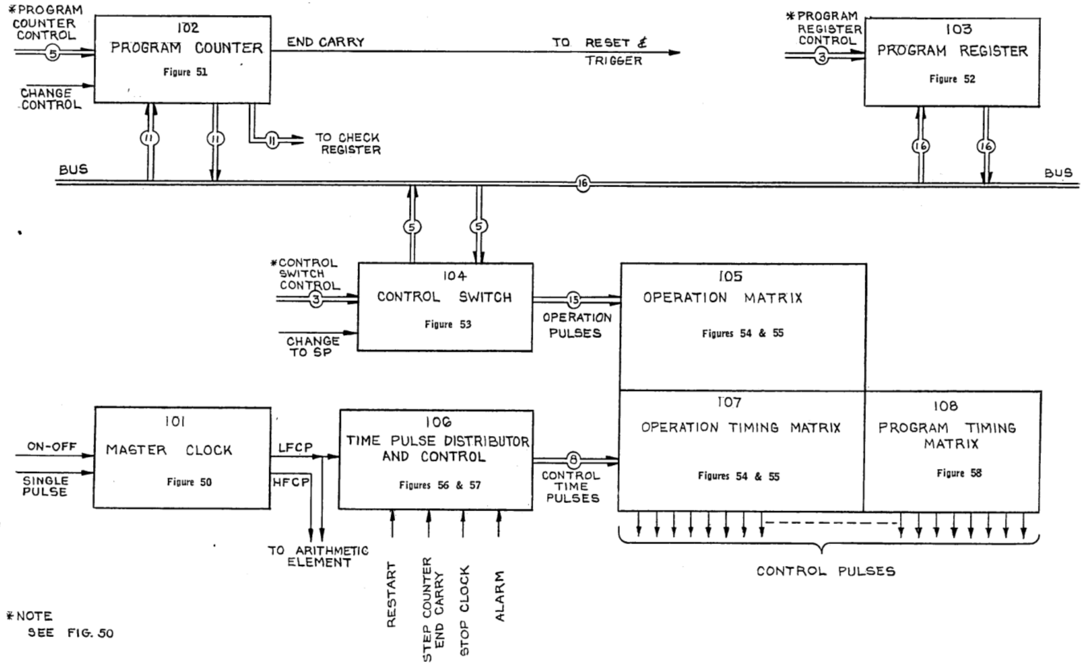
Whirlwind in R-127

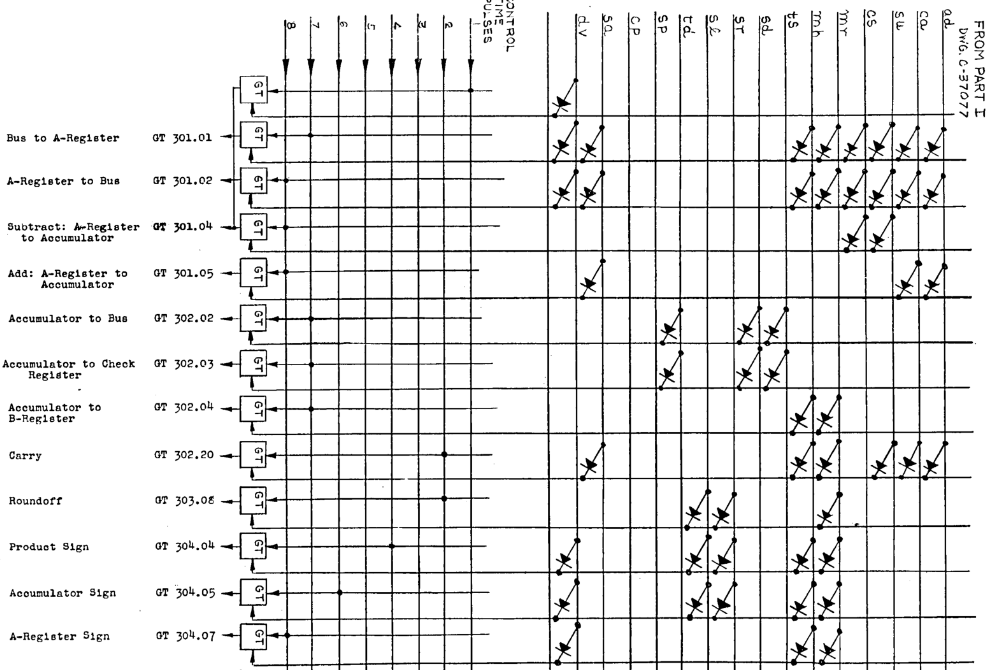
- Whirlwind I (prototype for Whirlwind II):
  - parallel
  - one's complement
  - 16 binary digits, fixed point (-1.0; 1.0), scale manually
  - up to 32 orders (instructions), 15 specified
  - up to 2048 words of electrostatic storage
  - 1 megacycle (Mhz), arithmetic faster
- Whirlwind II:
  - bigger numbers (40-46 digits)
  - more storage (640,000 digits = 14,000 - 16,000 words)
  - probably two orders per word (like IAS machine)
  - same speed
  - reality: plans changed, WW II became AN/FSQ-7
- no discussion of ES storage or IO equipment
- instead, test storage: 5 flip-flop words, 27 toggle-switch words

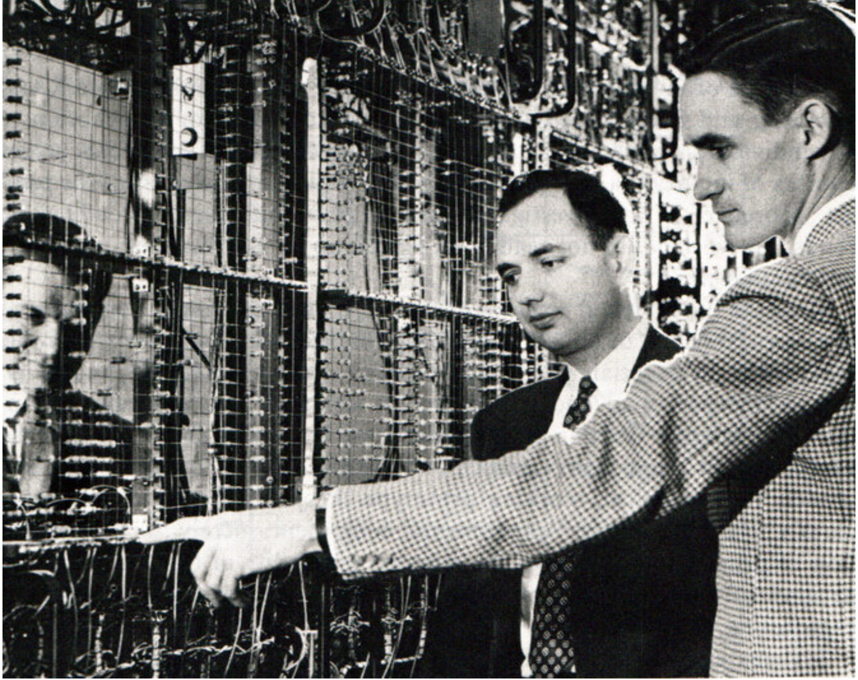
Orders in 1947

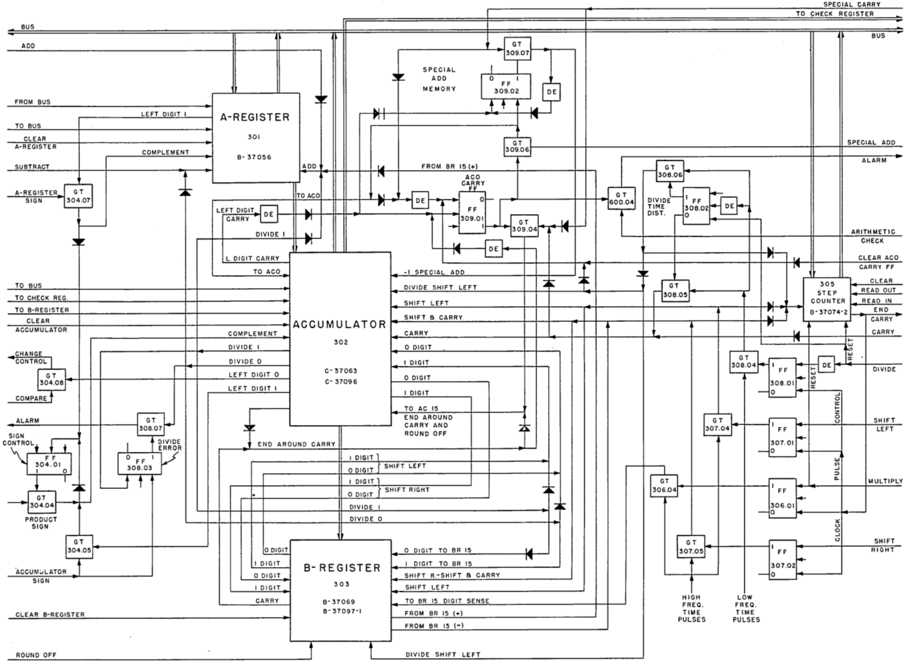
- 5 bits order, 11 bits address
- ca - clear and add - AC := Mem[addr]
- ad - add - AC := AC + Mem[addr]
- cs - clear and subtract - AC := -Mem[addr]
- su - subtract - AC := AC - Mem[addr]
- mh - multiply and hold - AC,BR := AC * Mem[addr]
- mr - multiply and round off - AC := round(AC * Mem[addr])
- dv - divide - BR := AC / Mem[addr]
- sr - shift right - AC,BR := AC,BR » n
- sl - shift left - AC,BR := AC,BR « n
- sp - subprogram - PC := addr
- cp - conditional subprogram - if AC > 0: PC := addr (later: <)
- ts - transfer to storage - Mem[addr] := AC
- td - transfer digits - Mem[addr] := AC (only address portion)
- sa - special add - like ad, but remember overflow
- sd - store and display - like ts, but display on scope (testing only)


PROGRAM COUNTER 102
PROGRAM REGISTER 103
STEP COUNTER 305
TOGGLE SWITCH STORAGE 202
FLIP-FLOP STORAGE 203
OUTPUT & DISPLAY 500
GT 102.02
GT 102.01
GT 102.03
GT 103.02
GT 103.01
GT 305.02
GT 305.01
GT 203.03
GT 203.02
GT 203.01
GT 500.01
BUS
BUS
GT 104.01
GT 104.02
GT 201.01
GT 201.02
GT 301.01
GT 301.02
GT 302.02
GT 302.03
GT 601.01
CONTROL SWITCH 104
STORAGE SWITCH 201
A REGISTER 301
ACCUMULATOR 302
CHECK REGISTER 601


*PROGRAM COUNTER CONTROL
102
PROGRAM COUNTER
Figure 51
END CARRY
TO RESET & TRIGGER
CHANGE CONTROL
TO CHECK REGISTER
*PROGRAM REGISTER CONTROL
103
PROGRAM REGISTER
Figure 52
BUS
BUS
*CONTROL SWITCH CONTROL
104
CONTROL SWITCH
Figure 53
CHANGE TO SP
OPERATION PULSES
105
OPERATION MATRIX
Figures 54 & 55
101
MASTER CLOCK
Figure 50
ON-OFF
SINGLE PULSE
LFCP
HFCP
TO ARITHMETIC ELEMENT
106
TIME PULSE DISTRIBUTOR AND CONTROL
Figures 56 & 57
CONTROL TIME PULSES
107
OPERATION TIMING MATRIX
Figures 54 & 55
108
PROGRAM TIMING MATRIX
Figure 58
CONTROL PULSES
RESTART
STEP COUNTER END CARRY
STOP CLOCK
ALARM
*NOTE SEE FIG. 50

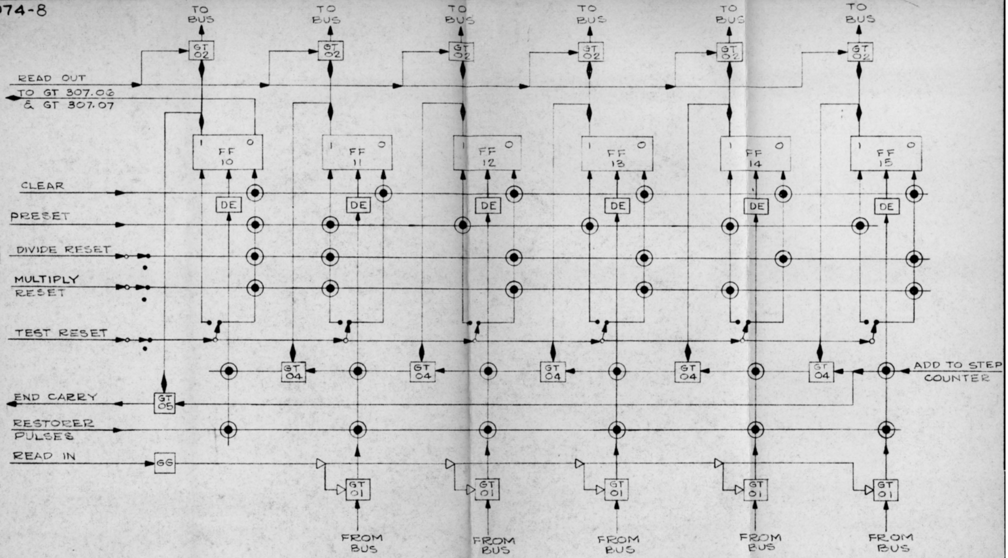

CONTROL TIME PULSES
FROM PART I DWG. C-37077
Bus to A-Register GT 301.01
A-Register to Bus GT 301.02
Subtract: A-Register to Accumulator GT 301.04
Add: A-Register to Accumulator GT 301.05
Accumulator to Bus GT 302.02
Accumulator to Check Register GT 302.03
Accumulator to B-Register GT 302.04
Carry GT 302.20
Roundoff GT 303.08
Product Sign GT 304.04
Accumulator Sign GT 304.05
A-Register Sign GT 304.07





SPECIAL CARRY
TO CHECK REGISTER
BUS
ADD
FROM BUS
TO BUS
CLEAR A-REGISTER
SUBTRACT
A-REGISTER SIGN
GT 304.07
LEFT DIGIT I
COMPLEMENT
A-REGISTER
301
B-37056
ADD
TO ACO
SPECIAL ADD MEMORY
GT 309.07
FF 309.02
DE
GT 309.06
FROM BR 15 (+)
ACO CARRY FF
FF 309.01
GT 309.04
GT 600.04
GT 308.06
DIVIDE TIME DIST.
FF 308.02
SPECIAL ADD
ALARM
ARITHMETIC CHECK
CLEAR ACO CARRY FF
LEFT DIGIT CARRY
DIVIDE I
L. DIGIT CARRY
TO ACO
TO BUS
TO CHECK REG.
TO B-REGISTER
CLEAR ACCUMULATOR
COMPLEMENT
DIVIDE I
DIVIDE O
LEFT DIGIT O
LEFT DIGIT I
ACCUMULATOR
302
C-37063
C-37096
-I SPECIAL ADD
DIVIDE SHIFT LEFT
SHIFT LEFT
SHIFT & CARRY
CARRY
O DIGIT
I DIGIT
O DIGIT
I DIGIT
TO AC 15
END AROUND CARRY AND ROUND OFF
GT 308.05
305 STEP COUNTER B-37074-2
CLEAR
READ OUT
READ IN
END CARRY
CARRY
RESET
DIVIDE
GT 308.04
FF 308.01
CONTROL
GT 307.04
FF 307.01
SHIFT LEFT
PULSE
MULTIPLY
GT 306.04
FF 306.01
CLOCK
GT 307.05
FF 307.02
SHIFT RIGHT
HIGH FREQ. TIME PULSES
LOW FREQ. TIME PULSES
CHANGE CONTROL
GT 304.08
COMPARE
ALARM
GT 308.07
DIVIDE ERROR
SIGN CONTROL
FF 304.01
FF 308.03
GT 304.04
PRODUCT SIGN
GT 304.05
ACCUMULATOR SIGN
END AROUND CARRY
I DIGIT
O DIGIT
SHIFT LEFT
I DIGIT
O DIGIT
SHIFT RIGHT
DIVIDE I
DIVIDE O
O DIGIT
I DIGIT
O DIGIT
I DIGIT
CARRY
B-REGISTER
303
B-37069
B-37097-1
O DIGIT TO BR 15
I DIGIT TO BR 15
SHIFT R.-SHIFT & CARRY
SHIFT LEFT
TO BR 15 DIGIT SENSE
FROM BR 15 (+)
FROM BR 15 (-)
CLEAR B-REGISTER
ROUND OFF
DIVIDE SHIFT LEFT

B-37074-8



NOTE: FF NUMBERS CORRESPOND TO BUS NUMBERS.

GRADED BY:	DATE:	THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
		GRADE I FOR REFERENCE ONLY
PRE	3-30-49	GRADE II PRELIMINARY DESIGN
		GRADE III FINAL DESIGN

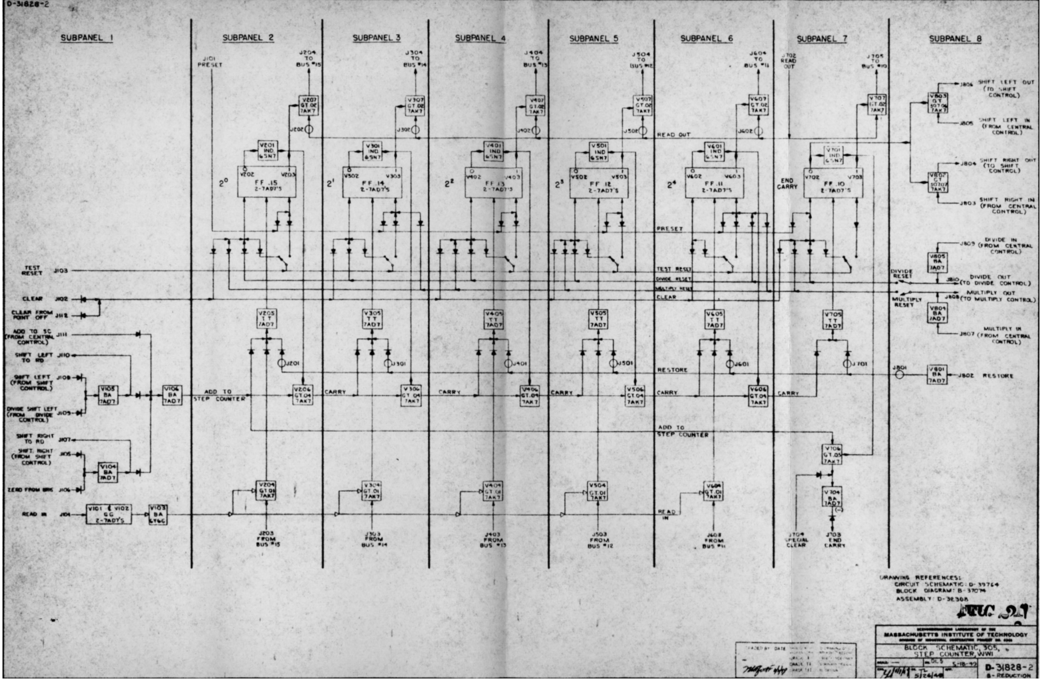
SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

BLOCK DIAGRAM, 305, STEP COUNTER, WWI

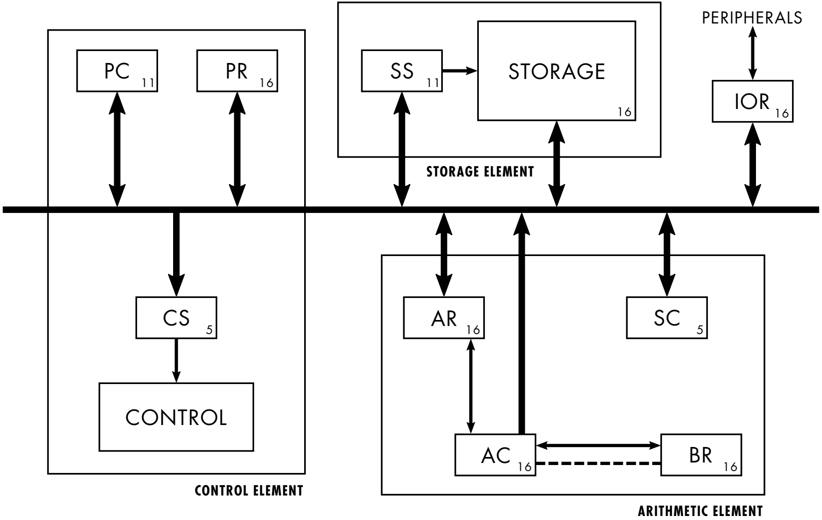
SCALE: — DR. JYa 2-25-48
ENG. 3/16/49 CK. APP.

B- 37074-8

FIG. 20


D-31828-2
SUBPANEL 1
SUBPANEL 2
SUBPANEL 3
SUBPANEL 4
SUBPANEL 5
SUBPANEL 6
SUBPANEL 7
SUBPANEL 8
J101 PRESET
J204 TO BUS #15
J304 TO BUS #14
J404 TO BUS #13
J504 TO BUS #12
J604 TO BUS #11
J702 READ OUT
J705 TO BUS #10
READ OUT
PRESET
TEST RESET
DIVIDE RESET
MULTIPLY RESET
CLEAR
RESTORE
CARRY
ADD TO STEP COUNTER
READ IN
END CARRY
TEST RESET J103
CLEAR J102
CLEAR FROM POINT OFF J112
ADD TO SC (FROM CENTRAL CONTROL) J111
SHIFT LEFT TO RD J110
SHIFT LEFT (FROM SHIFT CONTROL) J108
DIVIDE SHIFT LEFT (FROM DIVIDE CONTROL) J109
SHIFT RIGHT TO RD J107
SHIFT RIGHT (FROM SHIFT CONTROL) J105
ZERO FROM BRS J106
READ IN J104
V101 & V102 GG 2-7AD7'S
V103 BA 6Y6G
V104 BA 7AD7
V105 BA 7AD7
V106 BA 7AD7
FF 15 2-7AD7'S
FF 14 2-7AD7'S
FF 13 2-7AD7'S
FF 12 2-7AD7'S
FF 11 2-7AD7'S
FF 10 2-7AD7'S
J203 FROM BUS #15
J303 FROM BUS #14
J403 FROM BUS #13
J503 FROM BUS #12
J603 FROM BUS #11
J704 SPECIAL CLEAR
J703 END CARRY
J806 SHIFT LEFT OUT (TO SHIFT CONTROL)
J805 SHIFT LEFT IN (FROM CENTRAL CONTROL)
J804 SHIFT RIGHT OUT (TO SHIFT CONTROL)
J803 SHIFT RIGHT IN (FROM CENTRAL CONTROL)
J809 DIVIDE IN (FROM CENTRAL CONTROL)
J810 DIVIDE OUT (TO DIVIDE CONTROL)
J808 MULTIPLY OUT (TO MULTIPLY CONTROL)
J807 MULTIPLY IN (FROM CENTRAL CONTROL)
J801
J802 RESTORE
DRAWING REFERENCES:
CIRCUIT SCHEMATIC: D-39764
BLOCK DIAGRAM: B-37074
ASSEMBLY: D-32308
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
BLOCK SCHEMATIC, 305, STEP COUNTER, WWI
D-31828-2
8-REDUCTION

Whirlwind I block diagram

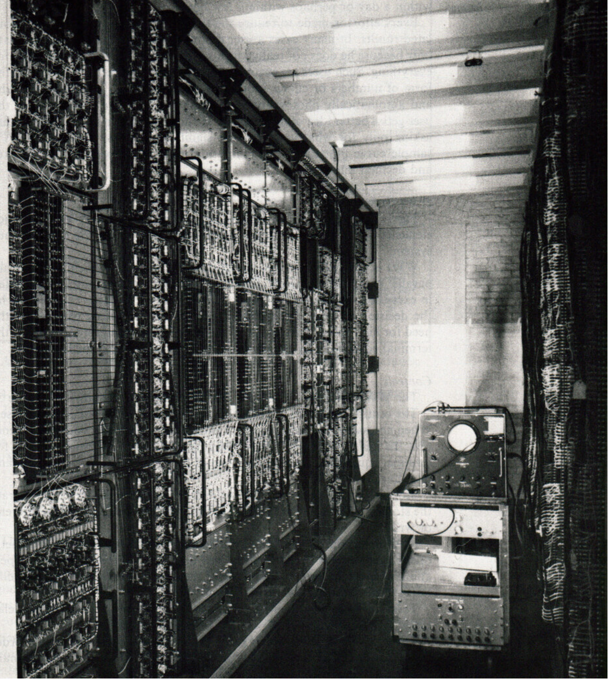


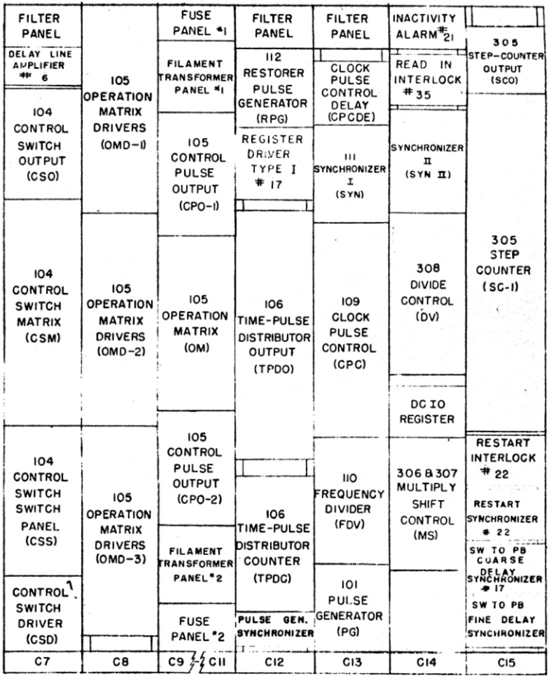
1948

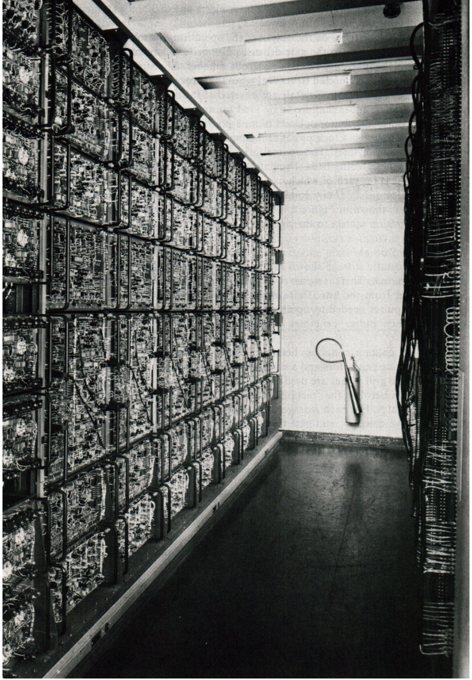
- point-off control added (normalize floating point numbers, sf)
- timing elements added and changed
- registers unified (AR and PR, BR and IO, CHECK and COMPARISON)
- matrices changed and combined
- sp now remembers return address in AR! ta added, most likely
- ao (add one) added
- sl* sr* proposed

1949

- IO orders explained and described
- first program runs on August 9th
- "the computer using test storage is essentially complete" (sept)
- solve and display differential equation on scope
- more orders proposed: qc (ck), qd/qh (display), qe (ex)




FILTER PANEL
DELAY LINE AMPLIFIER # 6
104 CONTROL SWITCH OUTPUT (CSO)
104 CONTROL SWITCH MATRIX (CSM)
104 CONTROL SWITCH SWITCH PANEL (CSS)
CONTROL SWITCH DRIVER (CSD)
105 OPERATION MATRIX DRIVERS (OMD-1)
105 OPERATION MATRIX DRIVERS (OMD-2)
105 OPERATION MATRIX DRIVERS (OMD-3)
FUSE PANEL #1
FILAMENT TRANSFORMER PANEL #1
105 CONTROL PULSE OUTPUT (CPO-1)
105 OPERATION MATRIX (OM)
105 CONTROL PULSE OUTPUT (CPO-2)
FILAMENT TRANSFORMER PANEL #2
FUSE PANEL #2
FILTER PANEL
112 RESTORER PULSE GENERATOR (RPG)
REGISTER DRIVER TYPE I # 17
106 TIME-PULSE DISTRIBUTOR OUTPUT (TPDO)
106 TIME-PULSE DISTRIBUTOR COUNTER (TPDC)
PULSE GEN. SYNCHRONIZER
FILTER PANEL
CLOCK PULSE CONTROL DELAY (CPCDE)
111 SYNCHRONIZER I (SYN)
109 CLOCK PULSE CONTROL (CPC)
110 FREQUENCY DIVIDER (FDV)
101 PULSE GENERATOR (PG)
INACTIVITY ALARM #21
READ IN INTERLOCK # 35
SYNCHRONIZER II (SYN II)
308 DIVIDE CONTROL (DV)
DC IO REGISTER
306 & 307 MULTIPLY SHIFT CONTROL (MS)
305 STEP-COUNTER OUTPUT (SCO)
305 STEP COUNTER (SC-1)
RESTART INTERLOCK # 22
RESTART SYNCHRONIZER # 22
SW TO PB COARSE DELAY SYNCHRONIZER # 17
SW TO PB FINE DELAY SYNCHRONIZER
C7
C8
C9 - C11
C12
C13
C14
C15



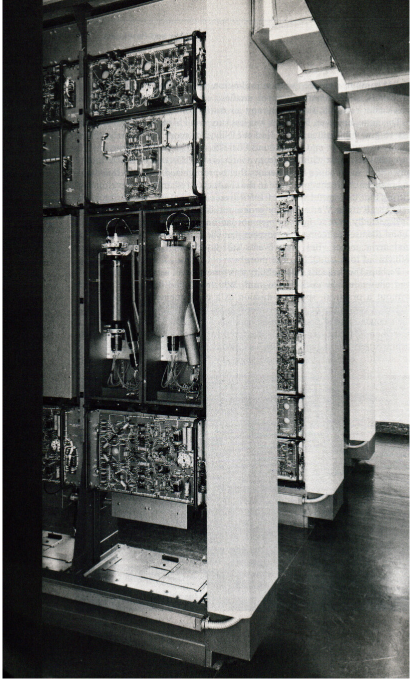
STANDARDIZER AMPLIFIER (SA-4)	BUS DRIVER (BD)	BUS DRIVER (BD)
ARITHMETIC ELEMENT DRIVER I (AED-1)	103 PROGRAM REGISTER (PR)	103 PROGRAM REGISTER (PR)
ARITHMETIC ELEMENT DRIVER I (AED-2)	102 PROGRAM COUNTER (PC)	102 PROGRAM COUNTER (PC)
ARITHMETIC ELEMENT DRIVER I (AED-3)	303 B-REGISTER (BR)	303 B-REGISTER (BR)
ARITHMETIC ELEMENT DRIVER I (AED-4)	302 ACCUMULATOR (AC)	302 ACCUMULATOR (AC)
ARITHMETIC ELEMENT DRIVER I (AED-5)		
ARITHMETIC ELEMENT DRIVER I (AED-6)	301 A-REGISTER (AR)	301 A-REGISTER (AR)
ARITHMETIC ELEMENT DRIVER I (AED-7)	601 CHECK REGISTER (CR-(9-15))	
AD	A8–A14	A15

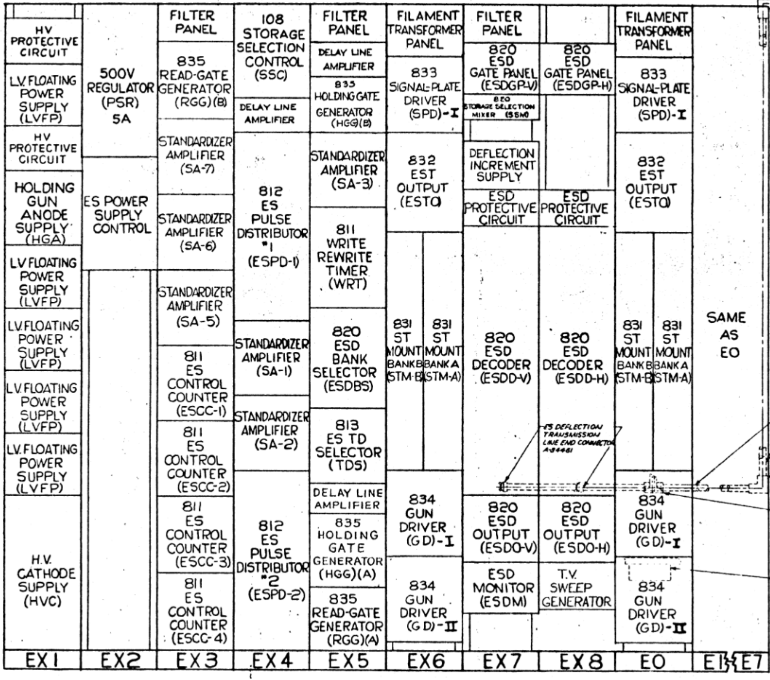
1950

- block diagrams in R-177
- PR removed for testing ES. AR taking its job temporarily
- qc/ck made canonical, more orders proposed
- IO system being integrated into WW
- work on magnetic core storage begins
- electrostatic storage integrated into WW
- first program runs from ES
- SRC (shift round-off control) proposed for sl* sr*

1950

- old IO system not flexible, new IO system considered
- first messages printed on flexowriter:
  "all ok
  will write
  more later
  love, WWI"
- SRC working
- Whirlwind ran reliably for a few hours




HV PROTECTIVE CIRCUIT
L.V. FLOATING POWER SUPPLY (LVFP)
HV PROTECTIVE CIRCUIT
HOLDING GUN ANODE SUPPLY (HGA)
LV FLOATING POWER SUPPLY (LVFP)
L.V. FLOATING POWER SUPPLY (LVFP)
L.V. FLOATING POWER SUPPLY (LVFP)
L.V. FLOATING POWER SUPPLY (LVFP)
H.V. CATHODE SUPPLY (HVC)
500V REGULATOR (PSR) 5A
ES POWER SUPPLY CONTROL
FILTER PANEL
835 READ-GATE GENERATOR (RGG) (B)
STANDARDIZER AMPLIFIER (SA-7)
STANDARDIZER AMPLIFIER (SA-6)
STANDARDIZER AMPLIFIER (SA-5)
811 ES CONTROL COUNTER (ESCC-1)
811 ES CONTROL COUNTER (ESCC-2)
811 ES CONTROL COUNTER (ESCC-3)
811 ES CONTROL COUNTER (ESCC-4)
108 STORAGE SELECTION CONTROL (SSC)
DELAY LINE AMPLIFIER
812 ES PULSE DISTRIBUTOR #1 (ESPD-1)
STANDARDIZER AMPLIFIER (SA-1)
STANDARDIZER AMPLIFIER (SA-2)
812 ES PULSE DISTRIBUTOR #2 (ESPD-2)
FILTER PANEL
DELAY LINE AMPLIFIER
835 HOLDING GATE GENERATOR (HGG)(B)
STANDARDIZER AMPLIFIER (SA-3)
811 WRITE REWRITE TIMER (WRT)
820 ESD BANK SELECTOR (ESDBS)
813 ES TD SELECTOR (TDS)
DELAY LINE AMPLIFIER
835 HOLDING GATE GENERATOR (HGG) (A)
835 READ-GATE GENERATOR (RGG)(A)
FILAMENT TRANSFORMER PANEL
833 SIGNAL-PLATE DRIVER (SPD)-I
832 EST OUTPUT (ESTO)
831 ST MOUNT BANK B (STM-B)
831 ST MOUNT BANK A (STM-A)
834 GUN DRIVER (GD)-I
834 GUN DRIVER (GD)-II
FILTER PANEL
820 ESD GATE PANEL (ESDGP-V)
820 STORAGE SELECTION MIXER (SSM)
DEFLECTION INCREMENT SUPPLY
ESD PROTECTIVE CIRCUIT
820 ESD DECODER (ESDD-V)
820 ESD OUTPUT (ESDO-V)
ESD MONITOR (ESDM)
820 ESD GATE PANEL (ESDGP-H)
ESD PROTECTIVE CIRCUIT
820 ESD DECODER (ESDD-H)
ES DEFLECTION TRANSMISSION LINE END CONNECTOR A-34461
820 ESD OUTPUT (ESDO-H)
T.V. SWEEP GENERATOR
FILAMENT TRANSFORMER PANEL
833 SIGNAL-PLATE DRIVER (SPD)-I
832 EST OUTPUT (ESTO)
831 ST MOUNT BANK B (STM-B)
831 ST MOUNT BANK A (STM-A)
834 GUN DRIVER (GD)-I
834 GUN DRIVER (GD)-II
SAME AS EO
EX1
EX2
EX3
EX4
EX5
EX6
EX7
EX8
EO
E1-E7

1951

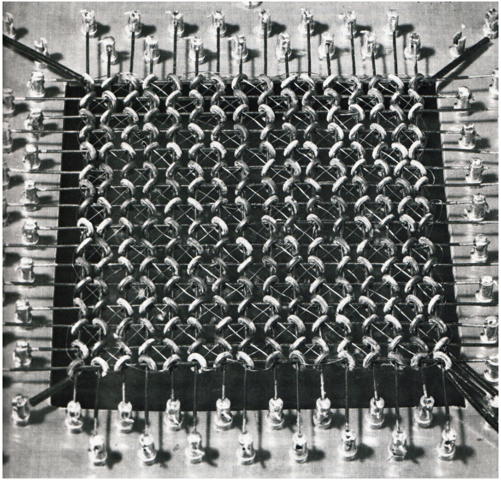
- no scans of bi-weekly reports :(
- work on IO system and ES continues
- Kodak-Eastman film units ditched
- ...

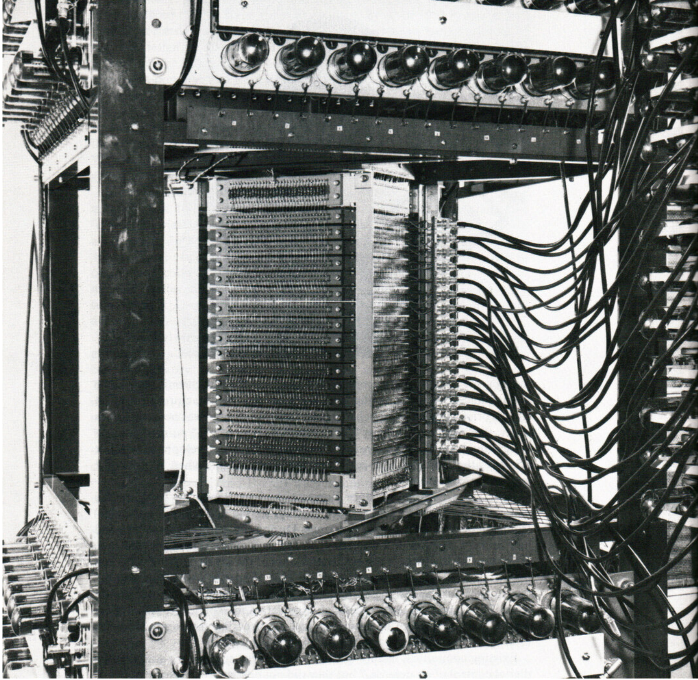
1952

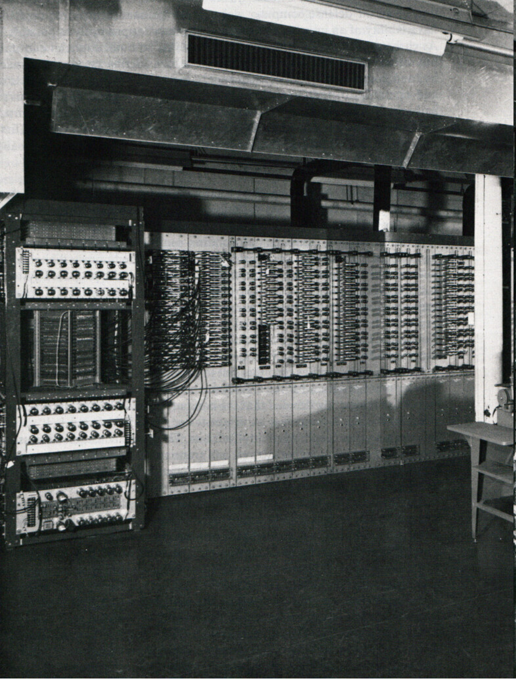
- ql/cl (cycle) discussed
- qe/ex made canonical
- 7-seg display constructed
- new IO system implemented
- PAR added, PR removed
- Memory Test Computer (aka WWIA, aka WWI½):
  - explore circuitry for WWII
  - test and bring up Magnetic Core Storage
  - various block diagrams and order codes discussed
  - final order code almost identical to Whirlwind I
  - construction much simpler by using test equipment
  - built by Ken Olsen (DEC) and Wesley Clark (TX-2, LINC)

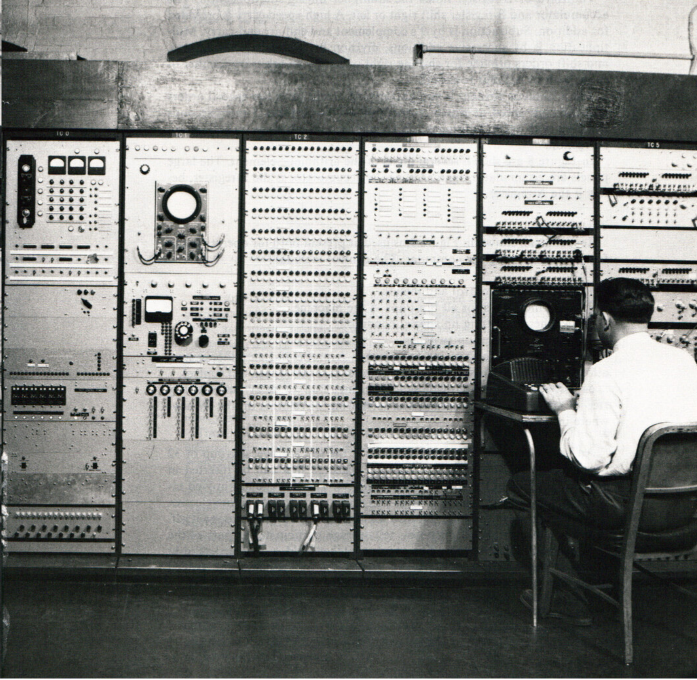
1953

- MTC:
  - registers tested calculates and plots sines and cosines (Minsky circle?)
  - MTC and core memory are working
- first bank of Core connected to Whirlwind
- second bank of Core connected to Whirlwind
- WWI now essentially in its final form








TC 0
TC 2
TC 5

Peripherals

- punch tape
- displays
- light guns
- flexowriters
- drum
- magnetic tape
- clock

Whirlwind's legacy

- new paradigm of computing:
  - real-time
  - interactive
  - computer part of a system, not merely a calculator
  - reliable
  - $\rightarrow$ beginning of the MIT tradition of computing
  - $\rightarrow$ DEC minicomputers
  - the first microcontroller?
- Core Memory, dominant type of memory for 2 decades
- WW II (aka AN/FSQ-7)
  - center piece of SAGE air defense system (22 SAGE sites)
  - built by IBM
  - IBM seriously enters the computer business
  - looks great in movies

Whirlwind I summary

INSTRUCTION			AC	BR	AR	SAM	C(x)
00000	SI	SELECT IO UNIT					
00001		ILLEGAL					
00010	BI	BLOCK IN	x + n		x		first word
00011	RD	READ	IOR		IOR		
00100	BO	BLOCK OUT	x + n		x		
00101	RC	RECORD					
00110	SD	SUM OF DIGITS	AC ∨ C(x)		C(x)	0	
00111	CF	CHANGE FIELDS					
01000	TS	TRANSFER TO STORAGE					AC
01001	TD	TRANSFER DIGITS					$C(x)_{0\text{-}4}, AC_{5\text{-}15}$
01010	TA	TRANSFER ADDRESS					$C(x)_{0\text{-}4}, AR_{5\text{-}15}$
01011	CK	CHECK					
01100	AB	ADD BR	BR + C(x)		C(x)	0	BR + C(x)
01101	EX	EXCHANGE	C(x)		C(x)		AC
01110	CP	CONDITIONAL SP			y+1		
01111	SP	SUBPROGRAM			y+1		
10000	CA	CLEAR, ADD	C(x) + SAM	0	C(x)	0	
10001	CS	CLEAR, SUBTRACT	−C(x) + SAM	0	C(x)	0	
10010	AD	ADD	AC + C(x)		C(x)	0	
10011	SU	SUBTRACT	AC − C(x)		C(x)	0	
10100	CM	CLEAR, ADD MAG.	$\lvert C(x)\rvert$+SAM	0	$\lvert C(x)\rvert$	0	
10101	SA	SPECIAL ADD	AC + C(x)		C(x)	±1 or 0	
10110	AO	ADD ONE	C(x) + 1		C(x)	0	C(x) + 1
10111	DM	DIFFERENCE OF MAG.	$\lvert AC\rvert - \lvert C(x)\rvert$	AC	$\lvert C(x)\rvert$	0	
11000	MR	MULTIPLY, ROUND	$(AC \times C(x))_{LT} + r$	0	$\lvert C(x)\rvert$	0	
11001	MH	MULTIPLY, HOLD	AC × C(x)	←	$\lvert C(x)\rvert$	0	
11010	DV	DIVIDE	±0	AC/C(x)	$\lvert C(x)\rvert$	0	
11011 0	SLR	SHIFT LEFT, ROUND	$(AC{:}BR \ll n)_{LT} + r$	0		0	
11011 1	SLH	SHIFT LEFT, HOLD	$AC{:}BR \ll n$	←		0	
11100 0	SRR	SHIFT RIGHT, ROUND	$(AC{:}BR \gg n)_{LT} + r$	0		0	
11100 1	SRH	SHIFT RIGHT, HOLD	$AC{:}BR \gg n$	←		0	
11101	SF	SCALE FACTOR	$AC{:}BR \ll n$	←	n	0	n
11110 0	CLC	CYCLE LEFT, CLEAR	$(AC{:}BR \text{ rot } n)_{LT}$	0			
11110 1	CLH	CYCLE LEFT, HOLD	AC:BR rot n	←			
11111	MD	MULTIPLY DIGITS	AC ∧ C(x)		−(final AC)		